מכללת טכנולוגיות הייטק

Board Design Academy - Marina Herzliya

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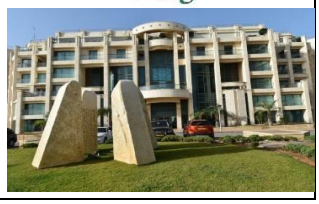

10 Days Course

Embedded System & Board design based Intel Architecture

Marina Herzliya by Shalom Shlomi Zigdon & Intel and Eastronics Lecturers

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Course Overview:

Embedded systems can be found in many industries segments including Artificial Intellegnet ,IoT , storage,communication/Telcom , automotive, militrary , transportation, agriculture, medical devices

Embedded system can be implemented by

- board design.
- Commercial off the Shelf (COTS) embedded modules & carrier board design .
- Commercial off the Shelf (COTS) embedded system.

In this course you will get the tools , challenges and complexity for each attitude.

Board design for smaller size, lesser weight, lower power, higher performance and faster speed has set the trend for multi-threaded and multi-core CPU based embedded design. Such design are associated with various challenges which will focus on this course and includes space constraints, trace routing constraints, length matching, signal integrity, power integrity, EMI/EMC constraints and thermal management.

The embedded systems engineering industry is showing an increasing demand for hardware and software engineers with a background in hardware Embedded modules focusing on **computer-on-module design**.

A computer-on-module (COM) is a type of single-board computer (SBC), a subtype of an embedded computer system. It is also called System-on-Module as an extension of the concept of System on Chip (SoC) and lying between a full-up computer and a microcontroller in nature.

The module will usually need to be mounted on a carrier board (or "baseboard") which breaks the bus out to standard peripheral connectors. We will focus in this course on COM carrier board design .

Who should attend:

This course is intended for technical professionals looking to acquire solid foundational knowledge necessary to design embedded systems focused on custom Board Design & Computer-On-Modules carrier board design .

The praticipation can be as following :

- Electronics engineers and Board layout engineers designing Computer-On-Modules carrier board for PICMG.
- Embedded Design Engineers
- FAE's support board design .
- hi-speed Board Designers
- System Enginner .
- HW system Architect .

Outcomes- What you will learn:

Students will learn definition and main components & modules of embedded systems, hardware design aspects, Commercial off the Shelf (COTS) embedded modules & systems , Embedded Computing Solution expert

Prerequisite:

Knowledge of electronic components and modules, reading and understanding electrical schematics.

Course Content

1. **Embedded system based Intel Architecture**
   - 1.1. Intel Architecture Introduction
   - 1.2. BIOS /Slim Bootloader
   - 1.3. Board Design based Intel Architecture
   - 1.4. Embedded Modules Form Factors focusing on COMe modules standard
   - 1.5. Embedded System
   - 1.6. Live Demo

2. **Why Security?**
   - **2.1. Security Vs Privacy**
   - 2.2. Intel Security Technologies Value Proposition
   - 2.3. Platform Integrity
   - 2.4. Intel® Boot Guard (Secure Boot)
   - 2.5. Protected Data, Key, ID
   - 2.6. Intel® Platform Trust Technology (Intel® PTT) &/or Discrete TPM (dTPM)
   - 2.7. Intel® Total Memory Encryption (Intel® TME)
3. **Crypto – Intel**
   - 3.1. Intel® AES-NI
   - 3.2. Intel® SHA Extensions
   - 3.3. Intel® Secure Key (DRNG)
4. **Trusted Execution**
   - 4.1. Intel® Software Guard Extensions (Intel® SGX)
   - 4.2. Intel® Virtualization Technology (Intel® VT)
   - 4.3. Intel® Total Memory Encryption- Multi Tenant* (Intel® TME-MT*)
5. **Scalability**
   - 5.1. WHAT IS SCALABILITY?
   - 5.2. Vertical vs. Horizontal
   - 5.3. SCALABILITY IN ELECTRONIC (HW) DESIGN
   - 5.4. THE BENEFIT – Cost for Scaling
   - 5.5. Typical scenarios for scaling
   - 5.6. Scaling within one product
   - 5.7. Scaling within product lines
6. **Main problems to challenge in hi-speed Carrier/Board design**
   - 6.1. Basic Fundamentals of Board Design
   - 6.2. The meaning of Signal Integrity for Board Designer
   - 6.3. Board Design vs. PCB Design
   - 6.4. Signal distortion Noise types
   - 6.5. Single Ended and Differential Signals
   - 6.6. Sources of Problems
7. **ElectroMagnetic Waves**
   - 7.1. What is a Wave really?
   - 7.2. Maxwell Equation in simple words
   - 7.3. Fourier Transform deep understanding

7.4. Moving from Kirchhoff & Ohms Laws to Maxwell Equations
7.5. The Spectrum of a Clock Signal
7.6. Harmonics structure of a Digital Random Signal

8. Theory Basic transmission line

8.1. Length of the Rising Edge – TEL Critical length, Fly time, Saturation length
8.2. Propagation Delay Time on External & Internal Layers
8.3. Tangent delta/ dissipation factor / Dielectric Absorption
8.4. Frequency Dependent Skin Effect, Skin depth calculation
8.5. Dielectric Losses of isolators tangent Delta Dissipation Factor
8.6. Signal Attenuation – Insertion losses

9. Return Current Path Possibilities

9.1. Rise time & Fall Time Switching Return Current
9.2. Return Current Path of Signal Closed to GND /VCC
9.3. Microstrip and Stripline difference of Signal propagation
9.4. Return current for a single-ended
9.5. The Stitching Via

10. The Impedance Meaning for Digital Signal

10.1. Characteristic Impedance of Conductor
10.2. Why 50 Ohm?
10.3. Stripline vs. Microstrip Calculation
10.4. Co-planar Waveguide

11. Saturn Calculators Training

11.1. Microstrip and Stripline Impedance
11.2. Conductor dimension for Current and Temperature
11.3. Conductors distance for Voltage difference

12. Reflections & Terminations

12.1. The physics of Reflection
12.2. The Impedance Matching
12.3. Reflection Coefficient and Lattice Diagram
12.4. When Termination is not a must
12.5. The Diodes and Active Terminations
12.6. ODT/OCT operation
12.7. Practical Tips for Terminations Placement
12.8. point to point, multi drop, star, tree, daisy chain
12.9. Routing Topology and Termination Strategies

13. **Crosstalk**

13.1. Conductors as 3D Antennas
13.2. Mechanism of Crosstalk, Capacitive and Inductive Coupling
13.3. NEXT and FEXT Crosstalk Diagram and Volume Calculation
13.4. Why inductive is stronger than Capacitive
13.5. PCB Layout Tips to reduce Crosstalk

14. EMI/EMC

14.1. EMI/EMC Theory & Terms
14.2. Common & Differential Mode radiation
14.3. Military and Industrial Standards
14.4. Faraday Cage Design in PCB
14.5. Layers Construction Copper Balance

14.6. 20H rule of Power Planes
14.7. The Best Multilayer construction for EMC

15. The Real world of Passive Component

15.1. The Capacitor Practical Model, ESR & ESL
15.2. Capacitor role as: Decoupling, Bypassing,
15.3. Filtering, Current Source, Bulk
15.4. The Inductor and Ferrit Bead Practical Model

16. Power Integrity Problems & Solutions

16.1. Ground Bounce/SSO/SSN
16.2. Total inductance and the return path
16.3. Design of Power Distribution Networks for High-speed Systems
16.4. Power Distribution Vias, Planes, Bypass Capacitors
16.5. Controlling parallel resonance peaks
16.6. Designing for Acceptable Ground Bounce/SSO/SSN
16.7. Return path control
16.8. Establishing target impedances

17. Capacitors and mounting

17.1. Capacitor value selection
17.2. Minimizing ground bounce in planes
17.3. VCC-GND planes tips to improve PDN by PCB Design

18. High speed serial links and differential pairs

18.1. Differential Pairs impedance
18.2. Termination strategies
18.3. Differential and common signals, even and odd mode impedances
18.4. Differential impedance, coupling and return currents
18.5. Routing rules

19. Channel Design for 5-40 Gbps

19.1. Frequency domain modeling of interconnections
19.2. Dissipation Factor of PCB Materials
19.3. Dielectric Losses of isolators
19.4. Via-Model and effects
19.5. Estimating the Total Inductance of Via
19.6. Laser Via-in-Pad and Backdrilling

20. Eye Pattern & Lossy Lines

20.1. Lossy Lines Fundamentals
20.2. Skin Effect of conductors – DC & AC Resistance
20.3. Dielectric Losses – Loss Tangent
20.4. the concept of the BER
20.5. Jitter Basics & Measurements
20.6. Causes of Random Jitter, Periodic Jitter, Data Dependent Jitter
20.7. Cycle-to-Cycle Jitter
20.8. TIE vs. Period Jitter vs. Cycle-to-Cycle
20.9. Advanced Oscilloscope Eye Pattern Measurement Demonstration
20.10. Copper Roughness influence

21. Lossy Line Considerations

- 21.1. Special PCB materials comparison
- 21.2. Pre-Emphasis & Equalization
- 21.3. Pre-Emphasis and De-Emphasis Solutions
- 21.4. Equalization Principles and Solutions
- 21.5. Tightly / Loosely Coupling Routing Rules

22. Multigiga Signals Routing rules

- 22.1. Multigigabit Differentials Communication Ethernet Versios Rules
- 22.2. PCIexpress Routing Rules
- 22.3. HDMI Versions for Video/Audio Signals
- 22.4. USB2 VS. USB3
- 22.5. Designing differential circuits
- 22.6. DDR2 VS. DDR3 VS. DDR4 ROUTING RULES
- 22.7. FPGA Design Rules
- 22.8. PCB LAYOUT DESIGN for Data & Address

23. Analog/POWER Designs

- 23.1. Design rules for Analog and Power Supply
- 23.2. Hi-Current Conductors Calculation
- 23.3. Hi-Voltage Conductors Calculation
- 23.4. Placement and Routing Rules for Analog PCBs

24. PCB Manufacturing Process

- 24.1. The Basic Materials type of basic
- 24.2. Terms: Onze, Clad, Tg, Td, CTE,
- 24.3. Glass-Epoxy Types FR4, FR406, FR408
- 24.4. Tangent Delta Dissipation Factor
- 24.5. Dielectric Losses of isolators
- 24.6. Tolerances of Dielectric Thickness
- 24.7. Influence of Electroplating on Impedance of Conductors
- 24.8. The Roughness
- 24.9. The Process: from Gerber to PCB
- 24.10. Test Coupon Types and purpose
- 24.11. The content of Gerber & Manufacturing File

25. Advanced new PCB Technologies

- 25.1. Embedded Resistors & Capacitors
- 25.2. HDI – Hi Density PCBs Design Options
- 25.3. Laser Vias types, Blind vs Buried
- 25.4. Staggered vs. Stucked microVias

26. Packages Types of ICs

- 26.1. The miniaturization Evolution
- 26.2. THT – SMT – Fine Pitch Tech
- 26.3. The BGA microBGA and CSP
- 26.4. Advantages and Disadvantages
- 26.5. Basic rules for Footprint Design

27. PCB Layers design

27.1. The Faraday Cage principle
27.2. Best Practice for 4-Layers, 6-Layers, 8-Layers, 10-Layers, 12-Layers
27.3. Routing rules for horizontal & vertical routing
27.4. The Stitching Via role
27.5. Multi voltages planes strategy
27.6. Power planes as EMI shielding

28. Components Placement strategies

28.1. Digital Board
28.2. Analog / Power Supply Board
28.3. Mixed Analog & Digital Board

29. Chassis Grounding Methods

30. **Thermal Management Design**

30.1. Radiation, Convection, Ventilation Heat Transfer Mechanisms
30.2. Heat spreader - cooling concept
30.3. Heat spreader with Passive/Active Heatsink
30.4. Heat spreader with Heat-Pipe to Chassis wall
30.5. Heat spreader to Chassis wall with Fins

31. High-Speed Carrier/Board Simulation and Measurements Demonstrations

31.1. Signal Integrity
31.2. Power Integrity
31.3. EMI RFI

32. Summary and Diplomas for Attendees